Master 2 Internship

Adapting Hardware Platforms to a Multi-Core Response Time Analysis Framework

VERIMAG Laboratory (Grenoble, France) 2024–2025
Team **"Shared Resources"**
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Context

Providing strong guarantees on the temporal bevahior of critical-systems is crucial in severous domains, such as avionics, aeronautics, automotive or nuclear. In order to do so, techniques have been developed to provide Worst-Case Execution Times (or WCET) of programs used in those critical systems, making it possible to bound the response time of the software on some processors – namely, on mono-core processors.
However, with the raising of multi- and many-core systems, it becomes more difficult to bound the response time of a given program, as it may interfere with other tasks at runtime. Analysis of the Worst Case Response Time (or WCRT) must hence consider not only the WCET of the task, but also the timing penalties that may occur due to the interferences of the other tasks (*e.g.,* cache and bus accesses, that may introduce unplanned delays). Last but not least, the analysis must also consider the hardware systems on which the software is being executed, as several aspects of the hardware can impact both the WCET and the interferences.
In this context, the Multicore Interference Analysis framework (or MIA) has been proposed in Verimag [1, 2]. This framework can be used to compute the WCRT of a given program, for a given hardware platform. Currently, it supports platforms based on standard features (*e.g.,* single-level round-robin arbitration, L1 cache, ...), as well as two generations of the MPPA[1]. The MPPA platforms exhibit interesting hardware features for WCRT analysis — namely, using configurable banked memories to limit interferences — which are not always available on other platforms.

Goals of the Internship

The goal of this internship is to study the impact of adding new hardware platforms to the MIA framework, in the context of the ANR project CAOTIC[2]. In particular, we wish to investigate how other complex platforms can be adapted to the banked memory model, to ease the modeling of interferences, as well as the development of critical applications.
In consequence, the following contributions are expected:

[1] **M**assively **P**arallel **P**rocessor **A**rray, a many-core processor from the Kalray company http://www.kalrayinc.com.

[2] **C**ollaborative **A**ctions **o**n **T**iming **I**nterferen**c**es, a research project funded by the **A**gence **N**ationale de la **R**echerche, led by Verimag.

- consider how those particular components might be configured to be used in critical-systems;
- propose new components from the literature, that would be interesting to analyze in the context of multi-/many-core based critical-systems;
- study how to model such components in the existing framework, adapting their behavior to the analysis. A particular focus will be put on communication and memory modeling, as they are the main sources of interferences in multi-/many-core systems.

Contributions are hence expected both on the theoretical aspects of the framework, and on the practical side, ideally leading to the implementation of new hardware platforms in the analysis framework.

Ideal Applicant

This internship proposal is for Computer Science students at M2 level/last year of engineering school[3]. The applicant must be proficient in the following knowledge/skills:

- micro-architecture of processors (*e.g.,* pipeline, cache policies, bus arbitration, ...)
- ability to read and understand research papers as well as technical documentation
- interest for verification methods (architecture modeling, WCET computation, ...)

As the MIA framework is written in `python`, good programming skills in this language would be appreciated.

Applications

To apply, send an email to claire.maiza@univ-grenoble-alpes.fr and bruno.ferres@univ-grenoble-alpes.fr, with your resume, a short covering letter, as well as any document that may support your application.

Location

The internship will take place in VERIMAG laboratory, located in the campus of Grenoble:

Laboratoire VERIMAG, Bâtiment IMAG,
150 place du Torrent,
38401 Saint-Martin-d'Hères

Biblio.

[1] M. Schuh, *Safe Implementation of Hard Real-Time Applications on Many-Core Platforms*. PhD thesis, Université Grenoble Alpes, 2022. Available at https://theses.hal.science/tel-03827333.

[2] H. Rihani, *Many-Core Timing Analysis of Real-Time Systems*. PhD thesis, Université Grenoble Alpes, 2017. Available at https://theses.hal.science/tel-01875711.

[3] Motivated applications at M1 level will also be considered.